7.5 to 11.5 GHz - 10W GaAs Power Amplifier

DATA SHEET **VWA 5000059 AA**

General Description

The VWA 5000059 AA is a 2 Stages analog High Power MMIC operating in the frequency range from 7.5 GHz to 11.5Ghz.
The device is a 2 stages cascaded amplifier designed in 0.25µm pHEMT process.
The device is capable of more than +40dBm saturated output power, and provides 25dB of small signal gain from 7.5GHz to 11.5GHz with less than +/- 1.5dB of gain variation. The design has been optimized to provide high efficiency, supply current is as low as 3.2A with +8V supply voltage, when delivering +40dBm output power.

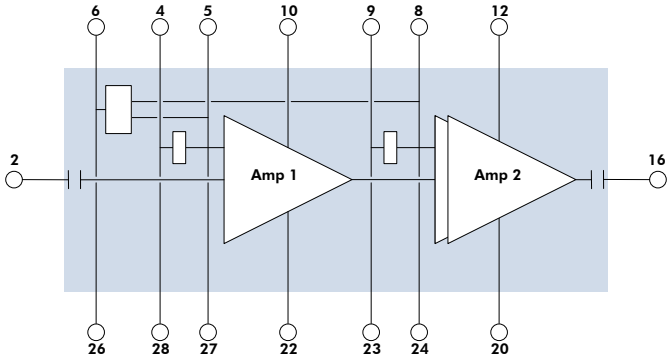
Features

- 2 Stages High Power pHEMT GaAs Amplifier
- Wide band: 7.5 to11.5GHz
- High Output P_{SAT} > +40dBm
- High Power Added Efficiency (PAE)>40%
- High P_{1dB} > + 39dBm
- High Small Signal Gain : 25dB
- 50Ω, AC coupled RF input and output access
- Power supply: 3.2A @ V_D = +8V; V_G=-0.8V
- Chip size : 4.4 x 2.5 x 0.1mm

Applications

- Radar
- Telecommunications
- X band High Power amplifier
- Test and measurement

Pins Assignement & Functional Block Diagram



Symbol	Pad N°
RF in	2
V_{SS}	6/26
V_{P1}	4/28
V_{G1}	5/27
V_{D1}	10/22
V_{P2}	9/23
V_{G2}	8/24
V_{D2}	12/20
RF out	16

Electrical Specifications

Test conditions unless otherwise noted :

- Tamb.= +25°C
- V_D Pulsed mode (Pulse width : 10µs, Duty cycle :10%)
- $V_D = V_{D1} = V_{D2} = +8V$
- $V_G = V_{G1} = V_{G2} = -0.8V$

Symbol	Parameter	Min	Typ	Max	Unit
F	Frequency Range	7		11.5	Ghz
BW	Operating Bandwidth		4.5		GHz
G	Small signal gain		25		dB
Pout	Output power @ Pin = +19 dBm		+40		dBm
PAE	Associated Power Added Efficiency @ Pin = +19 dBm	35	40		%
I_D	Supply current total ($I_D = I_{D1} + I_{D2}$)		3.2		A
ΔG	Small-signal Gain flatness		+/- 1.5		dB

Recommended Operating Conditions

- V_D Pulsed mode (Pulse width : 10µs, Duty cycle :10%)

Symbol	Parameter	Values	Unit
V_D	Drain Voltage	+8	V
V_G	Gate voltage	-0.8	V

Absolute Maximum Ratings

- V_D Pulsed mode (Pulse width : 10µs, Duty cycle :10%)

Symbol	Parameter	Min	Max	Unit
V_D	Drain Voltage without RF Input		8.5	V
V_G	Direct gate bias voltage	-3	0	V
V_{SS}, V_P	Gate bias voltage	-6	-4	V
I_D	Drain bias current ($I_D = I_{D1} + I_{D2}$)		4	A
Pin max	RF input power (peak)		+25	dBm

Care should be taken to avoid supply transient and over voltage. Over voltage above the maximum specified in absolute maximum rating section may cause permanent damage to the device.

Biasing options

Biasing access voltage values :

Pads name	Description	Voltage (V)	Current (A)
V_{D1}	First stage drain biasing access	8	$I_D = I_{D1} + I_{D2} = 3.2$
V_{D2}	Second stage drain biasing access	8	
V_{G1} ; V_{G2}	First stage and second stage gates direct biasing access	$-1 < V_G < -0.7$	$I_G = I_{G1} + I_{G2} = 0.07$
V_{P1} ; V_{P2}	First stage and second stage standard applications dedicated gates biasing access	-5	
V_{SS}	First stage and second stage compensated applications dedicated gates biasing access	-5	
Die bottom	DC and RF reference	0	

Gate access :

Depending on the applications environment, the gate of each stage can be biased using one of the three next options:

• Option 1:
Direct gate biasing (each stage individually, use V_{G1} and V_{G2}). This option is dedicated for device characterization period and high level of optimized amplifier functioning point.

• Option 2:
Gate biased through internal resistive voltage divider (use V_{P1} and V_{P2}). This option is more dedicated to standard and commercial applications.

• Option 3:
Gate biased using internal circuitry (use V_{SS}). This option is dedicated to a dispersion compensation need for particular applications.

Drain access :

The first stage drain can be biased on one side using pad V_{D1}.
The second stage drain need to be biased using the 2 pads V_{D2}.

DC Filtering access :

Parallel MIM capacitors must be placed on each used DC pads and on each V_{D1} access, in order to ensure the amplifier performances. Typically, a 100pF value in D20 format can be used. Also additional 10nF single layer capacitor is recommended on each bias connection.

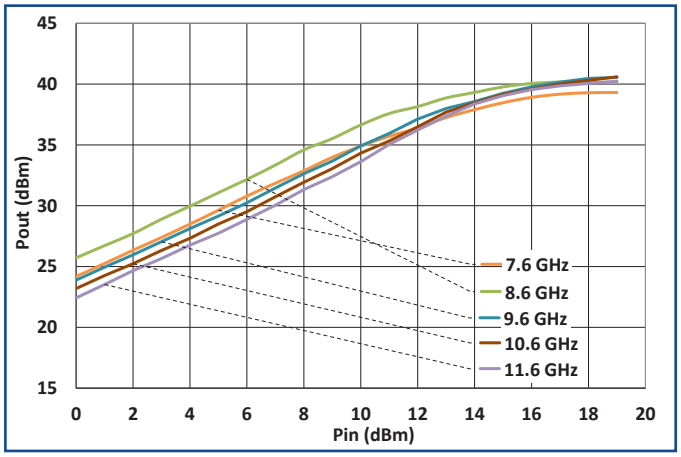
Typical Performance (Pulsed Mode / Test Under Probes)

Option 1

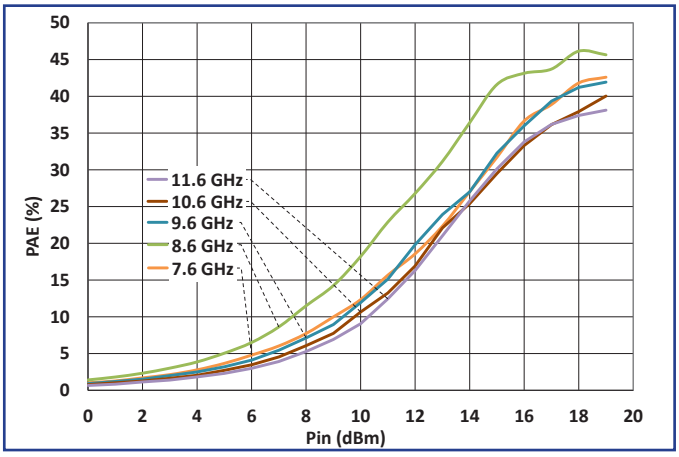
Test conditions: unless otherwise specified, test under probes

- Tamb.= +25°C
- $V_G = V_{G1} = V_{G2}$ = -0.8V
- V_D Pulsed mode (Pulse width: 10µs, Duty cycle: 10%)
- $V_D = V_{D1} = V_{D2}$ = +8V
- I_D = 3.2A

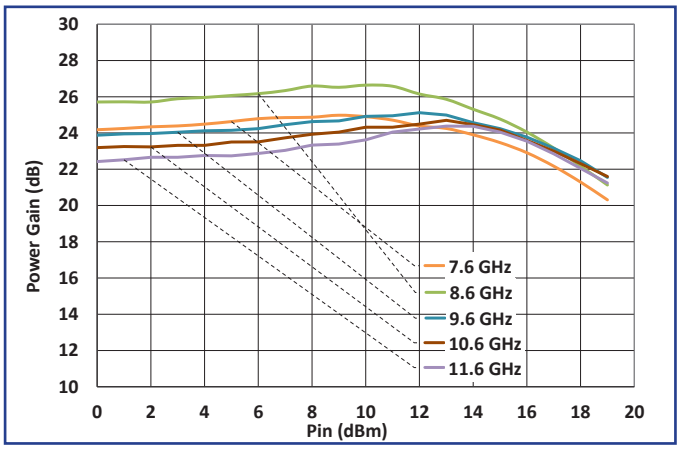
Output Power vs Input Power for various Frequency



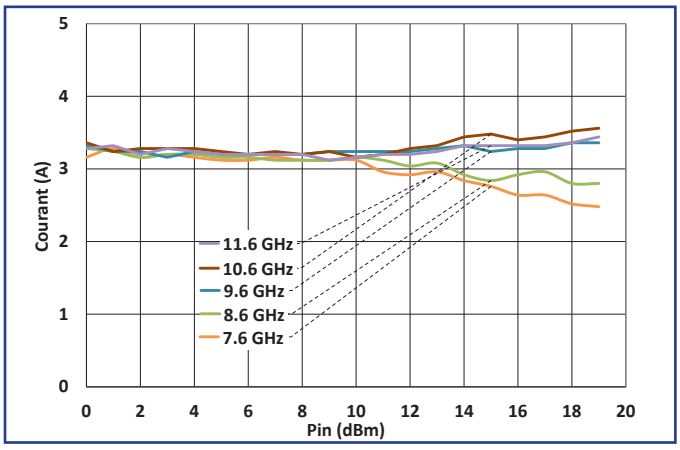
PAE vs Input Power for various Frequency



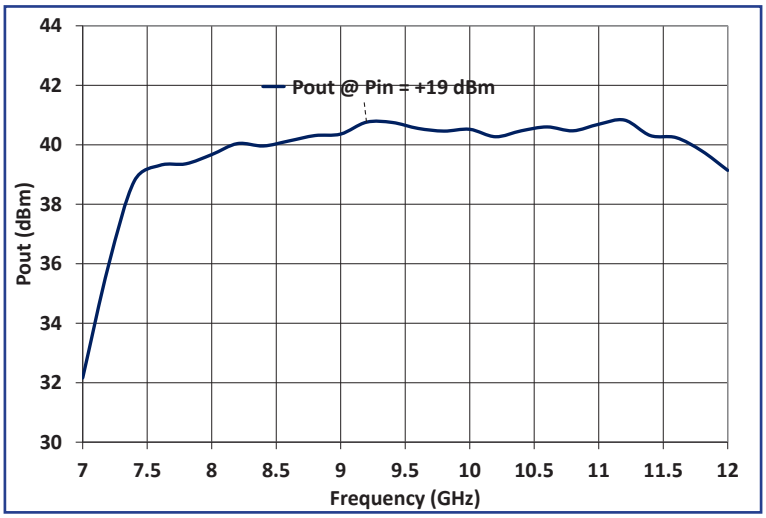
Power Gain vs Output Power for various Frequency



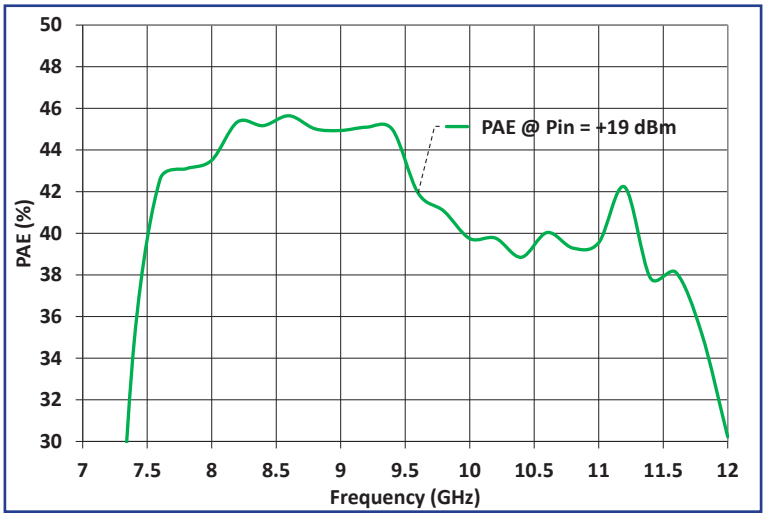
Drain Current vs Input Power for various Frequency



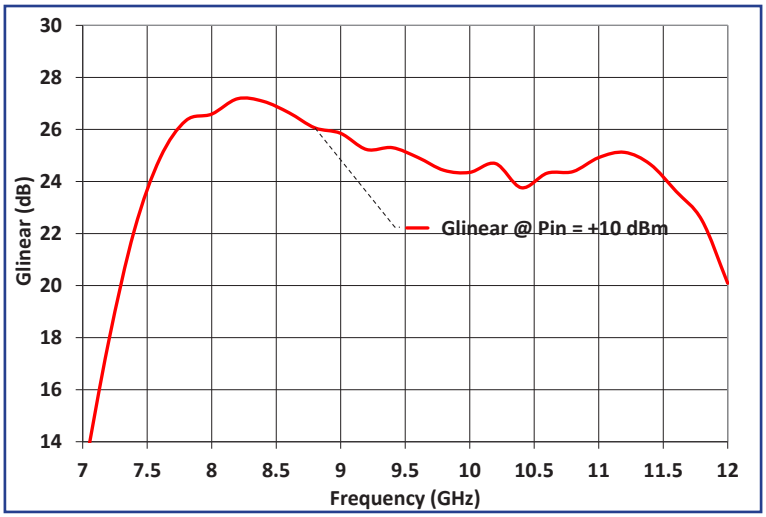
Output Power vs Frequency @ Pin = 19dBm



PAE vs Frequency @ Pin = 19dBm



Linear Gain vs Frequency @ Pin = 10dBm



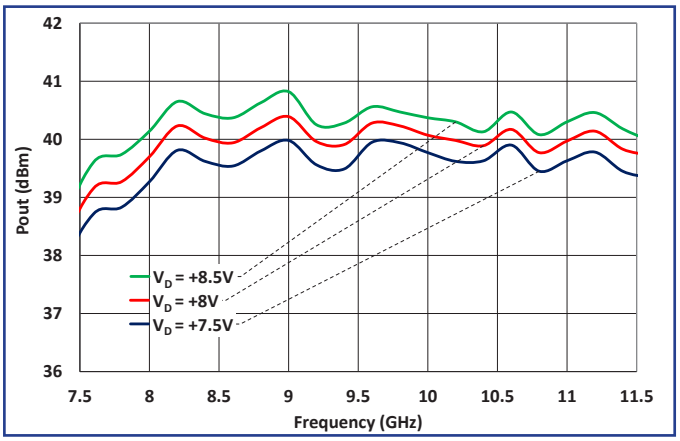
Additional measurement

Test conditions: unless otherwise specified, test under probes

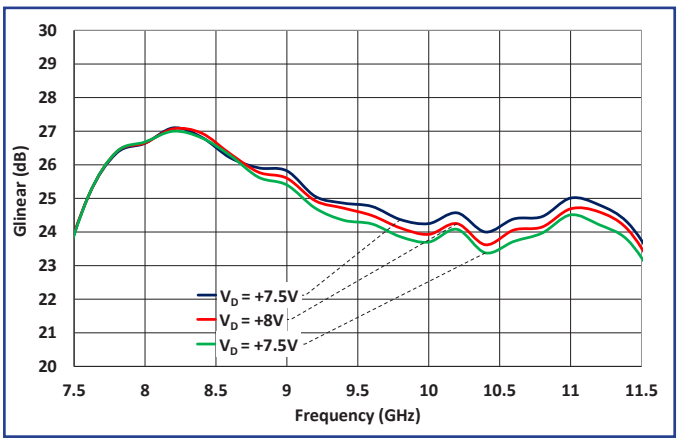
- Tamb.= +25°C
- V_D Pulsed mode (Pulse width: 10µs, Duty cycle: 10%)

Drain Voltage Variation for V_G = -0.8V

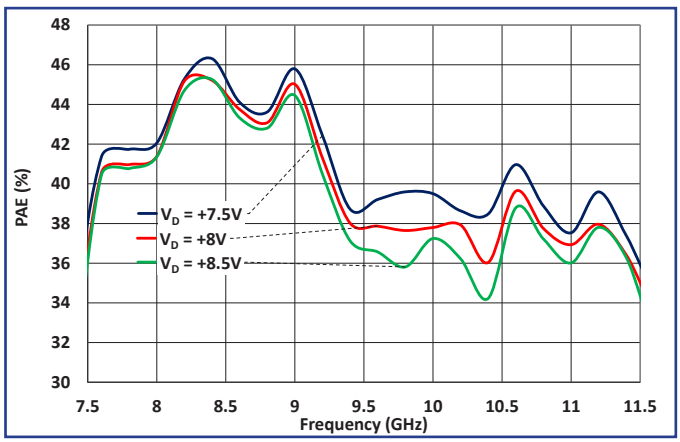
Output Power vs Frequency @ Pin = 19dBm



Linear Gain vs Frequency @ Pin = 10dBm

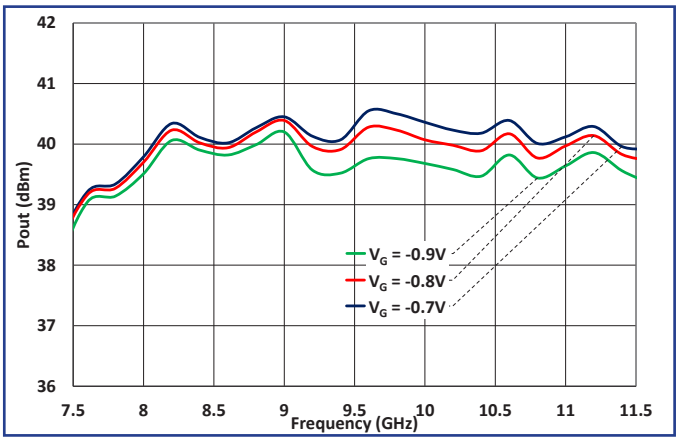


PAE vs Frequency @ Pin = 19dBm

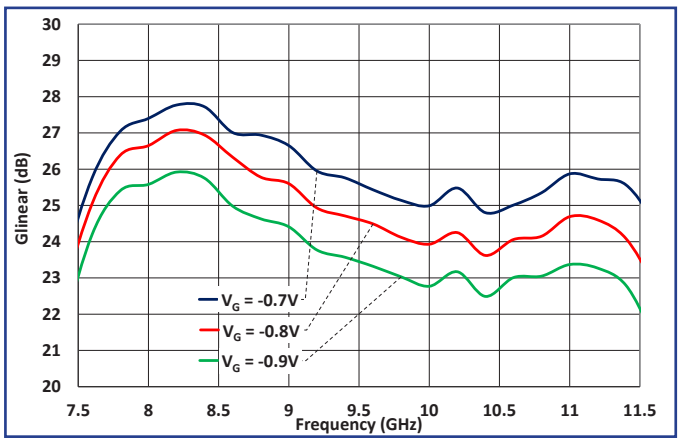


Gate Voltage Variation for V_D = +8V

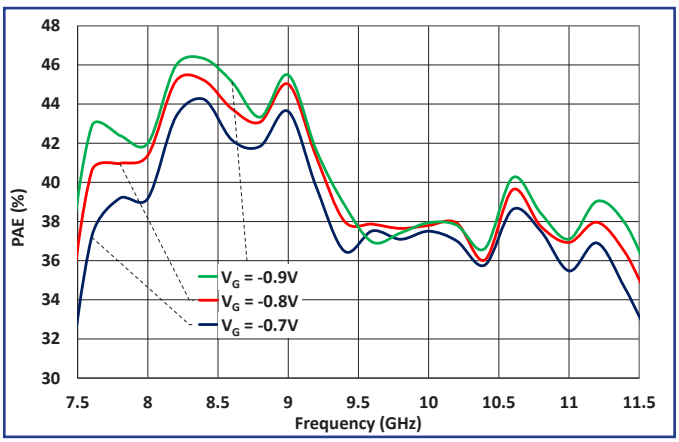
Output Power vs Frequency @ Pin = 19dBm



Linear Gain vs Frequency @ Pin = 10dBm

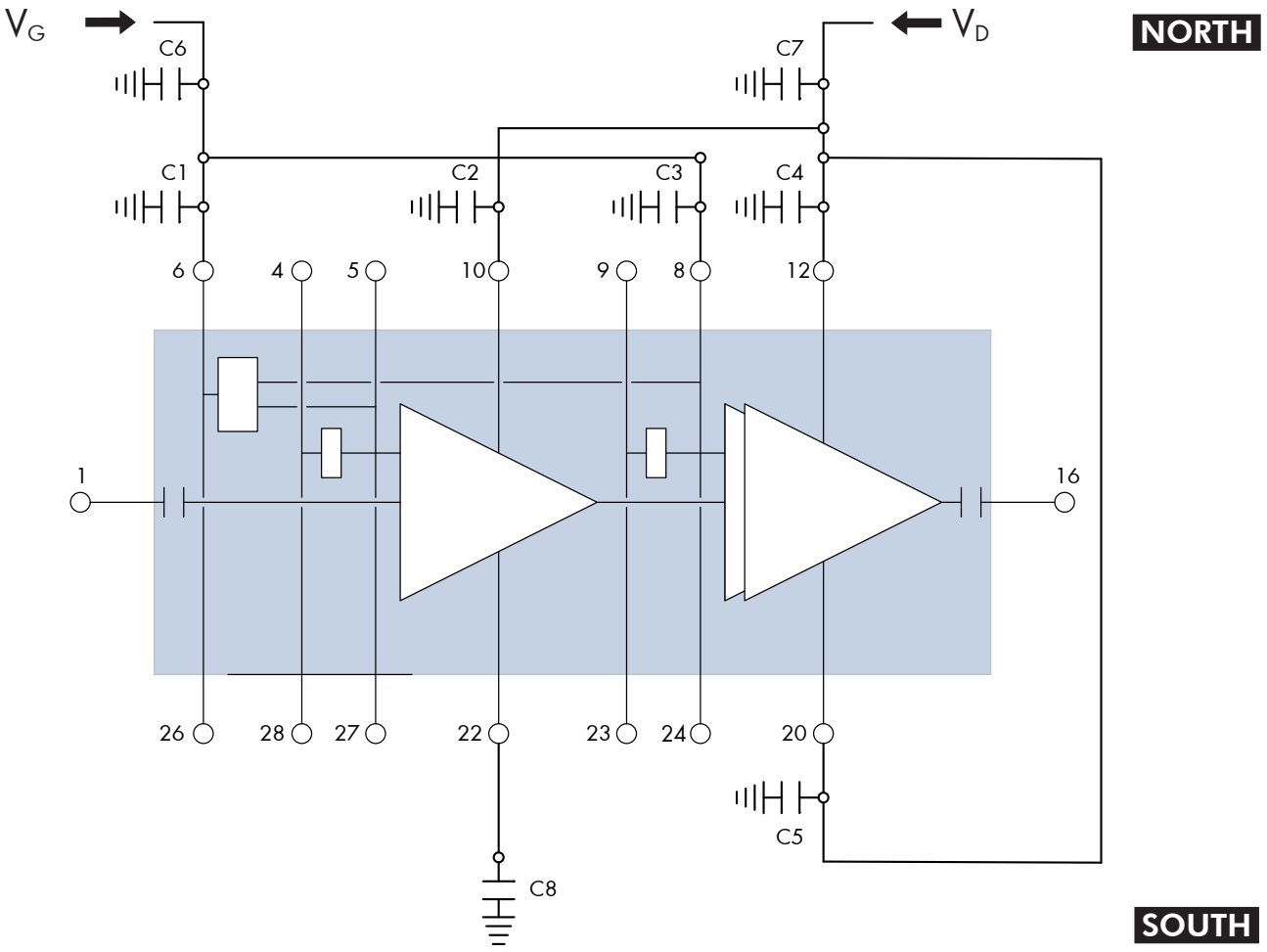


PAE vs Frequency @ Pin = 19dBm

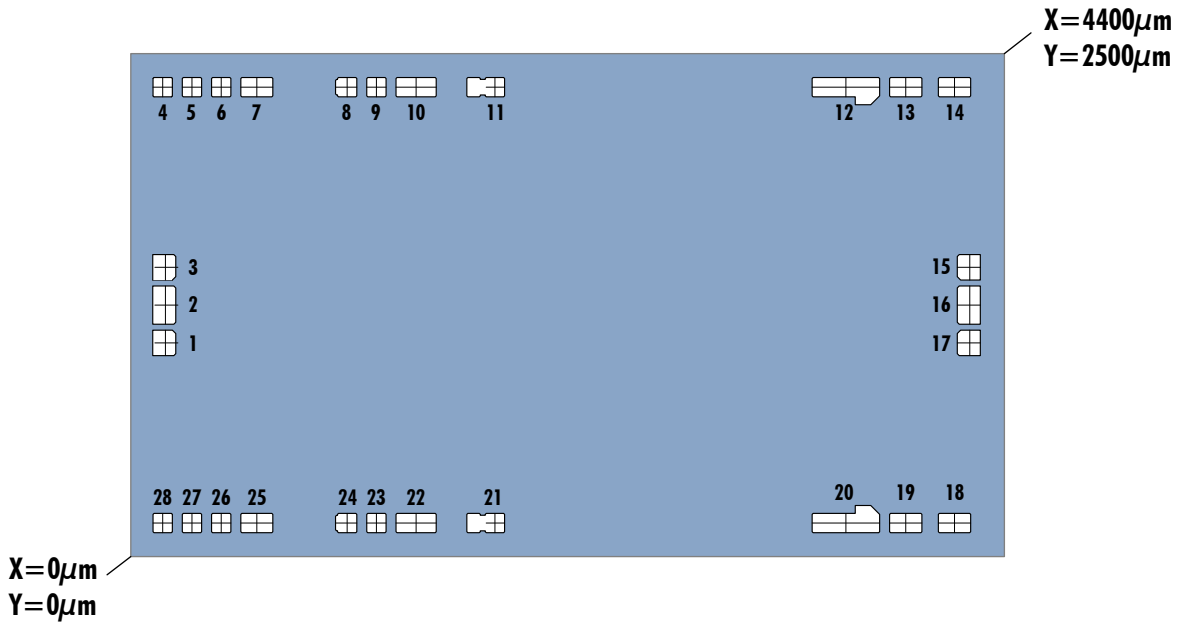


Application Circuit

- C1 to C5 = 100pF should be MIM capacitor
- C6 to C8 = 10nF



Die Layout



Pinout and Bonding Pad Coordinates

Die Pin Out				
Pad	**X (µm)**	**Y (µm)**	**Size (µm x µm)**	**Function**
1	125	1050	100x100	GND
2	125	1250	100x200	RF_Input : Ac Coupled
3	125	1450	100x100	GND
4	125	2368	100x100	V_{P1}_NORTH
5	275	2368	100x100	V_{G1}_NORTH
6	425	2368	100x100	V_{SS}_NORTH
7	580	2368	150x100	GND
8	1070	2368	100x100	V_{G2}_NORTH
9	1220	2368	100x100	V_{P2}_NORTH
10	1425	2368	200x100	V_{D1}_NORTH
11	1825	2368	150x100	GND
12	3570	2368	340x100	V_{D2}_NORTH
13	3900	2368	150x100	GND
14	4150	2368	150x100	GND
15	4275	1450	100x100	GND
16	4275	1250	100x200	RF_Output : Ac Coupled
17	4275	1050	100x100	GND
18	4150	132	150x100	GND
19	3900	132	150x100	GND
20	3570	132	340x100	V_{D2}_SOUTH
21	1825	132	150x100	GND
22	1425	132	200x100	V_{D1}_SOUTH
23	1220	132	100x100	V_{P2}_SOUTH
24	1070	132	100x100	V_{G2}_SOUTH
25	580	132	150x100	GND
26	425	132	100x100	V_{SS}_SOUTH
27	275	132	100x100	V_{G1}_SOUTH
28	125	132	100x100	V_{P1}_SOUTH

- Die thickness = 100µm
- Die bottom must be connected to ground (RF and DC)

Ordering Information

Product Code	Definition
VWA 5000059 AA	7.5 to 11.5 GHz 10 W

Associated Material

Material	Status
Packaged die	Contact factory
Die Evaluation Board (die EVB)	Contact factory
Packaged die Evaluation Board (packaged die EVB)	Contact factory
Mechanical files (DXF)	Contact factory
Measurents files (S2P)	Contact factory

Product Compliance Information

Solderability :

Use only AuSn (80/20) solder and limit exposure to temperature above 300 °C TO 3 - 4 minutes, maximum

ESD Sensitivy Rating :

Test : Human Body Model (HBM)
Standard : JEDEC Standard JESD22-A114

CAUTION ! ESD-Sensitive device

RoHS-Compliance :

This part is compliant with EU 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).
This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br402) Free
- PFOS Free
- SVHC Free

Contact Information

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